A COMPARISON OF ELECTRICAL PERFORMANCE ANALYSIS BETWEEN NANOSCALE DOUBLE-GATE AND GATE-ALL-AROUND NANOWIRE MOSFET

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This thesis is dedicated to my parents,
family and friends

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ABSTRACT

The Double-Gate and Gate-all-Around are said to be the promising candidates to pursue Complementary-Metal-Oxide Semiconductor scaling. When the device is scaled down, several problems arise such as the short-channel effect, excessive transistor gate leakage and power consumption. The purpose of this simulation work is to compare the performance of Double-Gate and Gate-All-Around and study the effect of scaling physical dimension on devices performance using Atlas Silvaco. It is found that when the gate length approaches 30 nm, the subthreshold slope increases for both devices while the threshold voltage is decreases. Futhermore, the threshold voltage will decrease with the decreasing of gate oxide thickness whilst increasing the silicon body thickness for both devices. Even though higher doping concentration is good for suppressing short channel effects, the lower doping concentration is desirable as both devices inhibit higher on-state currents. Gate-All-Around has greater value of current ratio compared to Double-Gate with 99.99% difference for low, light and heavy doping concentration. The gate dielectric materials play a significant role in the high performances of nanoscale devices. Different types of high dielectric constant material are used in order to study its influence towards Double-Gate and Gate-All-Around. The materials chosen in this study are Silicon Nitride, Aluminium Oxide, Zirconium Oxide and Hafnium Oxide. It can be observed that when approaching a higher value of dielectric constant, the on current, on-to-off current ratio and threshold voltage will increase while the subthreshold slope and off current will decrease. Hafnium Oxide shows the best performance compared to other simulated dielectric materials by having an improvement of leakage current with 98.64% and 73.85% when gate length approaching 30 nm for Double-Gate and Gate-All-Around respectively. Overall, Gate-All-Around offers a better continuous scaling down process compare to Double-Gate due to its efficient gate control, high current ratio, better short channel effect and subthreshold slope characteristics.

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ABSTRAK

Double-Gate dan *Gate-all-Around nanowire* adalah calon yang mempunyai harapan untuk meneruskan penskalaan transistor. Apabila saiz peranti berkurang, beberapa masalah timbul seperti kesan saluran pendek, kebocoran get transistor dan penggunaan kuasa yang berlebihan. Tujuan kerja simulasi ini adalah untuk membandingkan prestasi *Double-Gate* dan *Gate-all-Around* dan kemudian mengkaji kesan skala dimensi fizikal pada prestasi peranti menggunakan Atlas silvaco. Didapati bahawa pabila panjang get menghampiri 30 nm, cerun subambang meningkat untuk kedua-dua peranti manakala voltan ambang berkurangan. Selain itu, voltan ambang akan berkurangan dengan penurunan ketebalan get oksida dan peningkatan ketebebalan badan silikon untuk kedua-dua peranti. Kepekatan doping yang tinggi adalah baik untuk mengurangkan kesan jarak pendek namun kepekatan doping yang lebih rendah adalah wajar kerana kedua-dua peranti mempunyai arus mula yang lebih tinggi. *Gate-all-Around* mempunyai nisbah arus yang lebih besar berbanding *Double-Gate* degan perbezaan 99.99% untuk kepekatan rendah, ringan dan berat. Bahan get dielektrik telah memainkan peranan penting untuk prestasi tinggi untuk peranti nano. Pelbagai jenis bahan dielektrik tinggi telah digunakan untuk mengkaji pengaruhnya ke atas *Double-Gate* dan *Gate-all-Around nanowire*. Bahan dielektrik tinggi yang dipilih dalam kajian ini ialah Silikon Nitrida, Aluminium Oksida, Zirkonium Oksida dan Hafnium Oksida. Apabila menghampiri nilai pemalar dielektrik yang lebih tinggi, arus mula, nisbah arus dan voltan ambang akan meningkat sementara cerun subambang dan arus bocor akan berkurangan. Hafnium Oksida menunjukkan prestasi terbaik berbanding bahan-bahan dielektrik yang lain dengan peningkatan prestasi arus bocor sebanyak 98.64% dan 73.85% masing-masing untuk *Double-Gate* dan *Gate-all-Around*. Keseluruhannya, *Gate-All-Around* menawarkan proses penskalaan berterusan yang lebih baik berbanding *Double-Gate* kerana mempunyai kawalan get yang cekap, tingi nisbah arus, ciri-ciri kesan jarak pendek dan sub-ambang yang lebih baik.

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LIST OF SYMBOLS AND ABBREVIATIONS

2D	-	Two Dimensional
3D	-	Three Dimensional
3TADG	-	3 Tied-Gates Asymmetric Double-Gate
AC	-	Alternating Current
Al_2O_3	-	Aluminium Oxide
CB	-	Covalence Band
CMOS	-	Complementary Metal-Oxide Semiconductor
CDG	-	Common Double-Gate
DC	-	Direct Current
DIBL	-	Drain Induce Barrier Lowering
DG	-	Double-Gate
DMG	-	Dual-Material Gate
DMOS-DG	-	Dual Material Gate Oxide Stack Double-Gate
EOT	-	Effective Oxide Thickness
FET	-	Field Effect Transistor
GAA	-	Gate-All-Around
HCD	-	Hot-Carrier-Induced Degradation
HCI	-	Hot Carrier Injection
HfO_2	-	Hafnium Oxide
I_D	-	Drain Current
ITCs	-	Interface Trap Changes
ITRS	-	International Technology Roadmap Semiconductor
I_{off}	-	Off-State Current
I_{on}	-	On-State Current
K	-	Kappa
La_2O_3	-	lanthanum Oxide
LOP	-	Low Operating Power

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Lu_2O_3	-	Lutetium Oxide
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NMOS	-	N-type Metal Oxide Semiconductor
PMOS	-	P-type Metal Oxide Semiconductor
Q_{INV}	-	Inversion Carrier Sheet Density
Q_{TH}	-	Threshold Sheet Density
RDF	-	Random Dopant Fluctuation
SCE	-	Short Channel Effect
Sc_2O_3	-	Scandium Oxide
Si	-	Silicon
Si_3N_4	-	Silicon Nitride
SiO_2	-	Silicon Dioxide
SiGe	-	Silicon Germanium
SiNW	-	Silicon Nanowire
SGT	-	Single Gate Transistor
SOI	-	Silicon on Insulator
SS	-	Subthreshold Slope
TCAD	-	Technology Computer Aided Design
TMG	-	Tri-Material Gate
T_{si}	-	Silicon Thickness
T_{ox}	-	Oxide Thickness
VLSI	-	Very Large Scale Integration
V_{th}	-	Threshold Voltage
V_{dd}	-	Power Supply Voltage
VCP	-	Virtual Cathode Position
V_g	-	Gate Voltage
Y_2O_3	-	Yttrium Oxide
ZrO_2	-	Zirconium Oxide
μ	-	micro
ε_{si}	-	Dielectric of Silicon
ε_{ox}	-	Dielectric of Oxide
λ	-	natural length
α	-	alpha

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CHAPTER 1

INTRODUCTION

1.1 Limitation of Traditional MOSFET

Field-Effect Transistor (FET) is a type of device that has an amplification effect, characterize by low power requirements. The complementary metal-oxide semiconductor (CMOS) circuits widely used in computer nowadays are the combinations of a type of FET called metal-oxide-semiconductor field-effect-transistor, MOSFET. Applying voltage perpendicular to the surface of the semiconductor is used to control electrical transmission through the field effect.

Over the past of few decades, MOSFET also known as the centerpiece of microprocessor build with the memories belonged in the semiconductor industry. The need for high speed and great performance with low-cost device become the main reason why there are so many improvements and modification in transistor design. Numerous numbers of applications and great demand of a powerful microprocessor in a single chip become the main force to transistor designer to produce more reliable one. The focus is to place large number of transistors in a single chip while maintaining its reliability. Ever since the transistor is invented, the alterations are not something new to CMOS transistor as the innovation process keeps going on in order to fulfill the demand. As mention in the International Technology Roadmap for Semiconductors 2.0 (ITRS) 2015 [1], the crucial thing to be taken care of in high-performance device is the power consumption. Hence, the requirements of low power also apply in high performance transistor which is the basic component in the electronic device.

Note that the increment of transistor density in a device is possible when the size of the transistor is shrunk or squeezed them closer together [2]. Means that, when the size of transistor is getting smaller, the channel length is narrower and planar MOSFETs are not compatible anymore since more problems will arise. The

main problem when the gate control over the channel is not effective is the Short Channel Effect (SCE). Due to SCE, the increases of off-state current (I_{off}) with the degradation of subthreshold slope (SS) and threshold voltage (V_{th}) becomes prominent. These phenomena limit the performance of planar MOSFET [3].

Hence, the limitation of the planar MOSFET technology makes it nearly impossible to further scaling down or in other words increasing the number of the transistor. This situation is close enough with the prediction of Gordon Moore when he stated that the number of transistors incorporated in a chip will approximately double every 24 months and would eventually reach the limits of miniaturization at atomic levels [4]. Complying with Moore's law, it is already proved in practice today that conventional planar MOSFET technology has reached its full potential that means it is almost impossible to continue shrink beyond 20 nm without any costs [5].

1.2 New Transistor Structure

In order to improve the performance, reducing power dissipation is the crucial things need to be done otherwise future growth of semiconductor industry will be at risk. Instead of using planar MOSFET which is no longer can sustain to overcome the short-channel problem when approaching 20 nm node and beyond, a new structure design should be implemented to maximize the gate's control over the channel. In order to optimize the function and performance of the device, transistor designer or chip makers should concentrate on the physical and electrical characteristics of each device so that it can be fabricated with an optimum ability and best condition.

Recently, the new generation of MOSFET called multi-gate transistor structures is known to be the most suitable candidate to replace those planar structures. This new geometry will allow the continuous enhancement of electronic device performance to the next decade. The examples of multi-gate transistors are Double-Gate (DG), Triple-Gate, FinFET, Pi-Gate, Omega-Gate and Gate-All-Around (GAA) Silicon Nanowire (SiNW) MOSFET. All these transistors structure will give a different performance and its drawback.

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1.3 Problem Statement

High speed circuit, fast and low-power devices are a necessity for integrated circuit and become a high demand in the semiconductor industry. Hence, the desire to optimize the design metrics of functionality, performance and cost becomes more vigorous because there is always a room for innovation and improvement. In order to have advance functionality with the same area, smaller MOSFETs are preferable because more devices can fill up the chips. This is the reason of scaling down MOS devices have taken place.

When the conventional MOSFET is scaled down, several problems arise such as the SCE, channel length modulation, narrow channel effect and subthreshold conduction. Considering that planar MOSFET are no longer can sustain when manufacturing nodes progressed towards 20 nm and beyond, a new three dimensional (3D) structure was developed to overcome the limitation.

Problems related to SCE such as high leakage current, degradation of SS and Drain Induced Barrier Lowering (DIBL) making the planar MOSFET not compatible to further CMOS scaling. The reduction of device dimensions has lead to an alternative gate dielectrics replacing SiO_2 to suppress excessive transistor gate leakage and power consumption. SiO_2 layers thinner less than 2 nm would have a high leakage current due to direct tunneling through the oxide. Note that, DG was proposed after the planar MOSFET facing the problem related to SCE. Right after that, few multi-gate structures were invented such Triple-Gate, FinFET, and GAA MOSFET. Therefore, DG is the basic structure for multi-gate transistor while GAA is the latest structure. Hence, DG and GAA become the potential alternatives to overcome all the scaling issues. They have attracts researcher's attention due to its ability to suppress short channel effects and to overcome some of limitation faced by planar transistor even in smaller dimension.

This study focused on the performance analysis of Double-gate MOSFET and Gate-All-Around nanowire. By Using Silvaco Atlas TCAD tools, the simulation of the structure with parameter consideration is performed to get the device characteristics and configuration. The comparison of performance analysis between Double-gate and Gate-All-Around is done in order to know how much is the improvement from basic structure, DG to outstanding structure, GAA. Besides, the

comparison is made to study their properties under certain condition and which device has better performances in certain application such as in low or high power application.

1.4 Objectives of the Study

This study aims at fulfilling several objectives which are shown as below,

1. To simulate and characterize the electrical properties of Double-Gate and Gate-All-Around MOSFET with variation of physical dimension, doping concentrations and high-k dielectric material.
2. To investigate the effect of scaling down the dimension on electrical properties for Double-gate and Gate-All-Around MOSFET.
3. To analyze and compare the electrical performance between Double-Gate and Gate-All-Around MOSFET in terms of on-state current, off-state current, threshold voltage and subthreshold slope.

1.5 Scope of the Study

This study focuses on,

1. The electrical characterization of Double-gate and Gate-All-Around are using Atlas Silvaco TCAD tools.
2. The targeted electrical parameters for analytical analysis in this research are on-state current, off-state current, threshold voltage and subthreshold slope.
3. Silicon is used as substrate in the simulation structure.
4. Using Aluminium Oxide (Al_2O_3), Silicon Nitride (Si_3N_4), Hafnium Oxide (HfO_2) and Zirconium Oxide (ZrO_2) as the high-k dielectric materials.

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CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Recently, the new generation of MOSFETs called multiple gate transistor structures, are known to be the most suitable candidates to replace those planar structures because of their additional gate(s) [6]. These non-planar structures include the double-gate, tri-gate, FinFET, Pi-gate, Omega-gate and the latest one is called the Gate-All-Around MOSFET [7]. This new geometry will allow for the continuous enhancement of electronic device performances into the next decade. This transistor structure will give different levels of performance, and have its own drawbacks. The Gate-All-Around MOSFET becomes the best alternative among these existing structures, but the device's development is slightly challenging as the features have become more and more complex. It exists in nano-dimensions which need extra care to develop.

2.2 Scaling Issues: Short Channel Effects (SCEs)

The major challenge in the scaling down process of MOSFETs is the SCEs. The problems that arise due to short channeling include the increase of leakage current and the degradation of subthreshold slope and threshold voltage. SCEs also cause the increase of power consumption and eventually failing the transistor-switching action completely [8].

When the channel length decreases, the depletion regions linked with the source-to-body and drain-to-body regions become closer and start to interact with each other. Since depletion regions are regions of high electric fields, they facilitate carrier transport directly between the source-drain regions, which gives rise to the

observed phenomena of higher off-state currents, reduced threshold voltages and reduced control of the gate over transistor characteristics in MOSFETs [9].

In order to maintain Moore's Law and with research towards the invention of novel devices, short channel effects should be minimized. The short channel effects control generally depends on a scaling factor of the gate length and the natural length of the FET which can be written as in equation 2.1:

$$\alpha = \frac{L}{2\lambda} \tag{2.1}$$

Where:

α: scaling factor

L: gate length

λ: natural length/lambda

The natural length of the device, λ should be as small as possible as it is the measure of SCEs [10]. The natural length, λ is defined as in equation 2.2:

$$\lambda = \sqrt{\frac{\varepsilon_{Si}\, T_{Si} T_{ox}}{n T_{ox}}} \tag{2.2}$$

Where:

λ: natural length/lambda

ε_{Si}: permittivity of Si

ε_{ox}: permittivity of oxide

T_{si}: thickness of Si

T_{ox}: thickness of oxide

Besides that, the main scaling limiting factors are the different components of the leakage currents. For high-performance devices, all three major tunneling leakage currents (gate oxide, source-to-drain, and band-to-band tunneling of electrons or holes) will contribute to the ever-increasing power density of Very Large Scale Integration (VLSI) circuits. The reason is that the power supply voltage for high-performance devices is relatively higher than for the Low Operating Power (LOP)

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transistors. Therefore, controlling the leakage current in individual devices and designing power-optimized VLSI circuit architectures remain the main issue for research and development stages of the next generation devices.

2.2.1 Subthreshold Slope

Note that subthreshold slope is one of the crucial parameters during the short-channel immunity calculation of a device. Sub-threshold swing is basically the gate voltage needed to change for one decade of the drain current as shown in Figure 2.1.

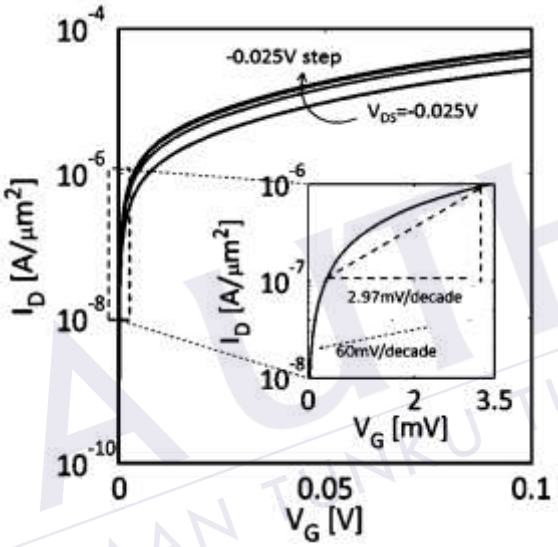

Figure 2.1: Subthreshold extraction from I_D-V_G curve [11].

It can be calculated by equation 2.3 [9]:

$$SS = \frac{\Delta V_G}{\log(\Delta I_D)} \tag{2.3}$$

Where:

SS: Subthreshold slope

V_G: Gate voltage

I_D: Drive current

In MOSFET, the ideal or tolerable value for the sub-threshold swing is 60mV/decade at ambient temperature [12]. A small subthreshold swing means better channel control, which shows the improvement of the I_{on}/I_{off} ratio, less leakage and less energy, so that it is good for a switching application [13], [14]. The values of the

threshold voltage and subthreshold slope are extracted from the I_D-V_G curve while the values for leakage current are from the I_D-V_D curve.

2.2.2 Threshold Voltage

As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. Scaling down the size of device meaning that the structure dimension also getting smaller. The structural dimensions refer to the channel length, oxide thickness, silicon film thickness. Threshold voltage can be varied with the changing of device dimension, body doping concentration [15]–[18]. To maintain performance, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available.

This phenomenon proves that threshold voltage, V_{th} of the MOSFET is a vital parameter in circuit design and testing, as well as in technology characterization where it should be used in whatever model adopted for the transistor. V_{th} signifies a physical change in the phenomenon that occur in the current flow through the device as it goes from weak to strong inversion [19].

Since this transition is very slow, no specific point can be directly identified as the threshold voltage in the current-voltage characteristic. For multi-gate devices, a threshold voltage is defined as the gate voltage at which the minimum inversion carrier sheet density, Qinv, reaches its threshold value which is required to turn on the device [20].

2.2.3 I_{on} / I_{off} Current Ratio

The on-to-off ratio indicates the merit for having high performance which is more on current, I_{on} and low leakage power (less I_{off}) for CMOS transistor . Typically more gate control leads to bigger I_{on} / I_{off} due to lower leakage current. When the transistor dimension is scaled down, the channel length becomes shorter as well and it will affect the gate control over the channel. For example when the thickness of SiO_2 that act as gate dielectric in both DG and GAA is scaled down, the direct tunneling will results in higher leakage current whilst decrease the I_{on} / I_{off} .

REFERENCES

[1] "International technology roadmap for semiconductor 2.0," 2015.

[2] K. Ahmed and K. Schuegraf, "Transistor wars," *IEEE Spectr.*, vol. 48, no. 11, pp. 50–66, 2011.

[3] Z. Johari and R. Ismail, "A review of Graphene based Field Effect Transistor architecture and channel geometry," *Sci. Adv. Mater.*, vol. 7, no. 10, pp. 2011–2020, 2015.

[4] G. E. Moore, "Cramming more components onto integrated circuits," *Proc. IEEE*, vol. 86, no. 1, pp. 82–85, 1998.

[5] G. Tshagharyan, G. Harutyunyan, S. Shoukourian, and Y. Zorian, "Overview study on fault modeling and test methodology development for FinFET-based memories," *Proc. 2015 IEEE East-West Des. Test Symp. EWDTS 2015*, pp. 9–12, 2016.

[6] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures," *Adv. Electron.*, vol. 2014, pp. 1–21, 2014.

[7] M. I. B. Chowdhury, M. J. Islam, M. J. Islam, M. M. Hasan, and S. U. Farwah, "Silvaco TCAD based Analysis of Cylindrical Gate -All-Around FET Having Indium Arsenide as channel and Aluminium Oxide as Gate Dielectrics," *J. Nanotechnol. its Appl. Eng.*, vol. 1, no. 1, pp. 1–12, 2016.

[8] L. GEPPERT, "The Amazing Vanishing Transistor Act," *IEEE Spectrum*, p. 33, 2002.

[9] V. Subramanian, "Multiple Gate Field-Effect Transistors for future CMOS technologies," *IETE Tech. Rev.*, vol. 27, no. 6, p. 446, 2010.

[10] C. Hu, "(Invited) FinFET and UTB--how to make very short channel MOSFETs," in *ECS Transactions*, 2012, vol. 50, pp. 17–20.

[11] A. Srivasta and M. Fahad, "A Graphene switching transistor for vertical circuit design," *ECS J. Solid State Sci. Technol.*, vol. 5, no. January, pp. M13–M21, 2016.

[12] X. Chen and C. M. Tan, "Modeling and analysis of Gate-All-Around Silicon

nanowire FET," *Microelectron. Reliab.*, vol. 54, no. 6–7, pp. 1103–1108, 2014.

[13] M. A. Abdi, F. Djeffal, D. Arar, and M. L. Hafiane, "Numerical analysis of Double Gate and Gate All Around MOSFETs with bulk trap states," *J. Mater. Sci. Mater. Electron.*, vol. 19, no. 1, pp. 248–253, 2008.

[14] S. Shee, G. Bhattacharyya, P. K. Dutta, and S. K. Sarkar, "Quantum confinement effects in the subthreshold characteristics of short-channel DMDG MOSFET," in *Proceedings of The 2014 International Conference on Control, Instrumentation, Energy and Communication (CIEC)*, 2014, pp. 122–126.

[15] B. Majkusiak, T. Janik, and J. Walczak, "Semiconductor thickness effects in the double-gate SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 45, no. 5, pp. 1127–1134, 1998.

[16] Y. Gu and J.Yuan, "Analysis on gate-oxide thickness dependence of hot-carrier-induced degradation in thin-gate oxide nMOSFET's," *IEEE Trans. Electron Devices*, vol. 33, pp. 1496–1503, 1990.

[17] Tsu-Jae King, Chenming Hu, J. Bokor, S. Tang, and L. Chang, "Gate length scaling and threshold voltage control of double-gate MOSFETs," in *IEDM*, 2002, no. 510, pp. 719–722.

[18] E. H. Minhaj and T. Dey, "Impact of channel length reduction and doping variation on multigate FinFETs," in *International Conference on Advancement in Electrical and Electronic Engineering*, 2018, no. December, pp. 99–103.

[19] O. Franca, M. C. Schneider, and C. Galup-montoro, "MOSFET threshold voltage : Definition, extraction, and some applications," *Microelectronics J.*, vol. 43, no. 5, pp. 329–336, 2012.

[20] R. Shankar, G. Kaushal, S. Maheshwaram, S. Dasgupta, and S. K.Manhas, "A degradation model of double gate and gate-all-around MOSFETs with interface trapped charges including effects of channel mobile charge carriers," *IEEE Trans. Device Mater. Reliab.*, vol. 14, no. 2, pp. 689–697, 2014.

[21] M. Veshala, R. Jatooth, and K. R. Reddy, "Reduction of short-channel effects in FinFET," *Int. J. Eng. Innov. Technol.*, vol. 2, no. 9, pp. 118–124, 2013.

[22] A. Sharma, "Performance analysis of gate-all-around field effect transistor for CMOS nanoscale devices," *Int. J. Comput. Appl.*, vol. 84, no. 10, pp. 44–48,

PTTA UTHM PERPUSTAKAAN TUNKU TUN AMINAH

2013.

[23] K. P. Pradhan, S. K. Mohapatra, P. K. Sahu, and D. K. Behera, “Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET,” *Microelectronics J.*, vol. 45, no. 2, pp. 144–151, 2014.

[24] A. A. Ziabari, M. Charmi, and H. R. Mashayekhi, “The impact of body doping concentration on the performance of nano DG-Mosfets: A quantum simulation,” *Chinese J. Phys.*, vol. 51, no. 4, pp. 844–853, 2013.

[25] S. Kumar, H. Pardeshi, G. Raj, and N. M. Kumar, “Superlattices and microstructures impact of gate length and barrier thickness on performance of InP/InGaAs based Double Gate Metal – Oxide-Semiconductor Heterostructure Field-Effect Transistor (DG MOS-HFET),” *Superlattices Microstruct.*, vol. 55, pp. 8–15, 2013.

[26] Sapna and B. Mehandia, “Study of electrical characteristics of SOI MOSFET using silvaco TCAD sSimulator,” *Curr. Trends Technol. Sci.*, vol. 1, no. 1, pp. 15–18, 2012.

[27] K. Chen, G. Zhang, and X. Zheng, “A subthreshold swing model for FD SOI MOSFET with vertical gaussian profile,” in *2011 International Semiconductor Device Research Symposium (ISDRS)*, 2011, pp. 1–2.

[28] N. Ashraf and D. Vasileska, “Static analysis of random telegraph noise in a 45-nm channel length conventional mosfet device: Threshold voltage and ON-current fluctuations,” *IEEE Trans. Nanotechnol.*, vol. 10, no. 6, pp. 1394–1400, 2011.

[29] P.Sahu, S. K. Mohapatra, and K. . Pradhan, “Performance of sub-100nm GS-DG MOSFET lastnosti pod-100 nm GS-DG MOSFET,” *J. Microelectron. Electron. Components Mater.*, vol. 44, no. 2, pp. 119–125, 2014.

[30] K. P. Pradhan, M. R. Kumar, S. K. Mohapatra, and P. K. Sahu, “Analytical modeling of threshold voltage for Cylindrical Gate All Around (CGAA) MOSFET using center potential,” *Ain Shams Eng. J.*, vol. 6, no. 4, pp. 1171–1177, 2015.

[31] K. Garg and D. Kapoor, “Single Gate Devices to Multigate Devices : A review,” *Int. J. Innov. Eng. Manag.*, vol. 4, no. 1, pp. 75–80, 2015.

[32] Hamid and R. Ismail, “Simulation of trigate FET with semi-cylindrical channel to reduce corner effect,” *IEEE Int. Conf. Comput. Model. Simul.*, vol.

15, no. 13, pp. 712–716, 2013.

[33] P. Razavi and A. A. Orouji, “Dual material gate oxide stack symmetric double gate MOSFET: Improving short channel effects of nanoscale double gate MOSFET,” *BEC 2008 - 2008 Int. Bienn. Balt. Electron. Conf. Proc. 11th Bienn. Balt. Electron. Conf.*, pp. 83–86, 2008.

[34] J. Park and J. Colinge, “Multiple-gate SOI MOSFETs: Device design guidelines,” *IEEE Trans. Electron Devices*, vol. 49, no. 12, pp. 2222–2229, 2002.

[35] M. Bhole, A. Kurude, and S. Pawar, “FinFET- Benefits, drawbacks and challenges,” *Int. J. Eng. Sci. Res. Technol.*, vol. 2, no. 11, pp. 2–5, 2013.

[36] S. K. Gupta, G. G. Pathak, D. Das, and C. Sharma, “Double gate MOSFET and its application for efficient digital circuits,” in *ICECT 2011 - 2011 3rd International Conference on Electronics Computer Technology*, vol. 2, pp. 33–36, 2011.

[37] A. Wagadre and S. Mane, “Design and performance analysis of DG-MOSFET for reduction of short channel effect over Bulk MOSFET at 20nm,” *Int. J. Res. Appl.*, vol. 4, no. 7, pp. 30–34, 2014.

[38] Prashant Mani and Manoj Kumar Pandey, “Silicon on insulator MOSFET development from single gate to multiple gate,” *Int. J. Adv. Res. Comput. Sci. Softw. Eng.*, vol. 2, no. 6, pp. 297–300, 2012.

[39] T. Dutta and S. Dasgupta, “Scaling issues in nanoscale double gate FinFETs with source/drain underlap,” *Comput. Devices Commun. 2009. CODEC 2009. 4th Int. Conf.*, pp. 2–5, 2009.

[40] R. Vaddi, R. P. Agarwal, S. Dasgupta, and T. T. Kim, “Design and analysis of double-gate MOSFETs for ultra-low power radio frequency identification (RFID): Device and circuit co-design,” *J. Low Power Electron. Appl.*, vol. 1, pp. 277–302, 2011.

[41] N. Sharan and S. Mahapatra, “A short-channel common double-gate MOSFET model adapted to gate oxide thickness asymmetry,” *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2732–2737, 2014.

[42] K. E. Kaharudin, A. H. Hamidon, and F. Salehuddin, “Impact of height of silicon pillar on vertical DG-MOSFET device,” *Int. J. Comput. Inf. Eng.*, vol. 8, no. 4, pp. 647–651, 2014.

[43] B. Yu, H. Lu, M. Liu, and Y. Taur, "Explicit continuous models for double-gate and surrounding-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2715–2722, 2007.

[44] B. Jena, B. S. Ramkrishna, S. Dash, and G. P. Mishra, "Conical surrounding gate MOSFET: A possibility in gate-all-around family," *Adv. Nat. Sci. Nanosci. Nanotechnol.*, vol. 7, no. 1, 2016.

[45] D. Jiménez *et al.*, "Continuous analytic I-V model for surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 571–573, 2004.

[46] Y. Jiang *et al.*, "Performance breakthrough in 8 nm gate length gate-all-around nanowire transistors using metallic nanowire contacts," in *IEEE Symposium on VLSI Technology Digest of Technical Papers*, pp. 34–35, 2008.

[47] S. D. Suk *et al.*, "High performance 5nm radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk si wafer, characteristics, and reliability," in *IEDM Tech. Dig. IEEE international*, 2005, pp. 717–720.

[48] V. Pott, K. E. Moselund, D. Bouvet, L. De Michielis, A. M. Ionescu, and S. Member, "Fabrication and characterization of gate-all-around silicon nanowires on bulk silicon," *IEEE Trans. Nanotechnol.*, vol. 7, no. 6, pp. 733–744, 2008.

[49] C. Mohan, S. Choudhary, and B. Prasad, "Gate all around FET: An alternative of FinFET for future technology nodes," *Int. Adv. Sci. Eng.*, vol. 6, no. 7, pp. 561–569, 2017.

[50] P. Zheng, D. Connelly, F. Ding, and T. J. K. Liu, "FinFET evolution toward stacked-nanowire FET for CMOS technology scaling," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 3945–3950, 2015.

[51] J. Y. Song, W. Y. Choi, J. H. Park, J. D. Lee, and B. G. Park, "Design optimization of gate-all-around (GAA) MOSFETs," *IEEE Trans. Nanotechnol.*, vol. 5, no. 3, pp. 186–190, 2006.

[52] H. Chen, Y. Wu, and C. Chang, "Performance of GAA poly-Si nanosheet (2nm) channel of junctionless transistors with ideal subthreshold slope," in *Digest of Technical Papers - Symposium on VLSI Technology (2013) ISSN: 07431562*, 2013, vol. 96, pp. 2012–2013.

[53] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Effect of channel & gate engineering on Double Gate (DG) MOSFET-A comparative study," *2012 Int.*

Conf. Emerg. Electron. ICEE 2012, pp. 4–6, 2012.

[54] Y. Chai *et al.*, "Low-resistance electrical contact to carbon nanotubes with graphitic interfacial layer," *IEEE Trans. Electron Devices*, vol. 59, no. 1, pp. 12–19, 2012.

[55] M. Shrivastava *et al.*, "On the thermal failure in nanoscale devices: Insight towards heat transport including critical BEOL and design guidelines for robust thermal management & EOS/ESD reliability," in *IEEE International Reliability Physics Symposium Proceedings*, pp. 342–346, 2011.

[56] L. Zhang, J. He, F. Liu, J. Zhang, and Y. Song, "A unified charge-based model for symmetric DG mosfets valid for both heavily doped body and undoped channel," in *15th International Conference, MIXDES 2008*, pp. 367–372, 2008.

[57] B. Iñíguez *et al.*, "Explicit continuous model for long-channel undoped surrounding gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1868–1873, 2005.

[58] V. Kumar, R. Gupta, R. Preet, P. Singh, and R. Vaid, "Performance analysis of double gate n-FinFET using high-k dielectric materials," *Int. J. Innov. Res. Sci. Eng. Technol.*, vol. 5, no. 7, pp. 13242–13249, 2016.

[59] T. Yamashita *et al.*, "Opportunities and challenges of FinFET as a device structure candidate for 14nm node CMOS technology," *ECS Trans.*, vol. 34, no. 1, pp. 81–86, 2011.

[60] V. Kumar, P. C. Samuel, D. M. Thomas, and M. Kumar, "Analysis of dual gate MOSFETs using high k dielectrics," in *2011 3rd International Conference on Electronics Computer Technology*, 2011, vol. 1, pp. 22–25.

[61] R. Chaudhary, R. Mukhiya, G. Singh, P. R. Mudimela, and R. Sharma, "Simulation of MOSFET with Different Dielectric Films," *2018 Int. Conf. Intell. Circuits Syst.*, pp. 173–176, 2018.

[62] P. Charles, D. Nirmal, P. P, S. Altrin, and M. M.Anuja, "Impact of gate length on the performance of a junctionless dual metal transistror with High-K dielectrics," in *Interational Conference on Devices, Circuits and Systems (ICDCS'16)*, pp. 7–10, 2016.

[63] J. Robertson and R. M. Wallace, "High-K materials and metal gates for CMOS applications," *Mater. Sci. Eng. R Reports*, vol. 88, pp. 1–41, 2015.

PTTA UTHM PERPUSTAKAAN TUNKU TUN AMINAH

[64] G. K.Saramekala, S. Dubey, and P. K.Tiwari, “A threshold voltage model of short-channel fully-depleted recessed-source/drain (Re-S/D) SOI MOSFETs with high-k dielectric,” *Chinese Phys. B*, vol. 24, no. 10, p. 8, 2015.

[65] N. Chatterjee, K. Chopra, K. Bhatia, and S. Pandey, “Finite element analysis of silicon gate all around nanowire transistor with different high-k dielectrics,” *IEEE Region 10 Annual International Conference, Proceedings/TENCON*. IEEE, pp. 1–5, 2016.

[66] D. Duggal and R. N. Sharma, “Review article on analytical models for single gate and double gate MOSFETs in subthreshold regime,” *Int. Conf. Microelectron. Comput. Commun. MicroCom 2016*, 2016.

[67] M. Gupta and A. Nandi, “Impact of matched high-k gate dielectric based DG-MOSFET on SRAM performance,” in *4th International Conference on Power, Control and Embedded Systems, ICPCES 2017*, pp. 1–5, 2017.

[68] J. Robertson, “High dielectric constant oxides,” *Eur. Phys. J. Appl. Physics.*, vol. 291, no. 28, pp. 265–291, 2004.

[69] M. Olyaei, “Low-frequency noise in high-k gate stacks with interfacial layer engineering" Doctoral Thesis in Information and Communication Technology KTH Royal Institute of Technology Stockholm, Sweden,” 2015.

[70] M. Chakraverty, “Simulation of electrical characteristics of Gate All around Silicon Nanowire Field Effect Transistor using extended Hückel theory based semi empirical approach,” *IOSR J. Electron. Commun. Eng.*, vol. 01, no. 01, pp. 148–154, 2016.

[71] B. R. Kumar and T. S. Rao, “High-k gate dielectrics of thin films with its technological applications – A review,” *Int. J. Pure Appl. Sci. Technol.*, vol. 4, no. 2, pp. 105–114, 2011.

[72] J. J. Gu *et al.*, “20-80nm channel length InGaAs Gate-All-Around nanowire MOSFETs with EOT=1.2nm and lowest SS=63mV/dec,” in *Technical Digest - International Electron Devices Meeting, IEDM*, pp. 633–636, 2012.

[73] M. Chan *et al.*, “Modeling the floating-body effects of fully depleted, partially depleted, and body-grounded SOI MOSFETs,” *Solid. State. Electron.*, vol. 48, no. 6, pp. 969–978, 2004.

[74] C. K. Maiti, S. Chattopadhyay, and L. K. Bera, “Strained-Si heterostructure

field effect devices," CRC Press, p. 155, 2007.

[75] R. Gupta, D. Dass, R. Prasher, and R. Vaid, "Impact of Silicon Body Thickness on the Performance of Gate-all-around Silicon Nanowire Field Effect Transistor," in *Physics of Semiconductor Devices*, Springer, pp. 689–692, 2014.

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